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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,033	07/10/2003	Lixin Zhao		6392

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Lixin Zhao
43454 Bryant St.
Fremont, CA 94539

EXAMINER

BREWSTER, WILLIAM M

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicant(s)

10/619,033

Applicant(s)

ZHAO, LIXIN

Examiner

William M. Brewster

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11, 13 and 14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11, 13 and 14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

Claims 9, 11, 13, 14 are objected to because of the following informalities: end of sentence punctuation is nonexistent or incorrect. Appropriate correction is required.

The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 13 and 14 should be renumbered 12 and 13. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee, GP Publication No. 2,240,429 A.

Lee anticipates a method of forming an image sensor, comprising: in fig. 6, starting a substrate N- sub, with a first conductive type of semiconductor material; and

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forming a semiconductor layer on the substrate, P-EPI Layer, which has a second conductive type; and the second conductive type is opposite to the first conductive type and a PN junction is formed in the interface;

limitations from claim: 3, further comprising: forming a photodiode element, the photodiode element PD having a first well region, N+, of said first conductive type formed in said second conductive type semiconductor layer, a second well region, P+, of said second conductive type formed in said second conductive type semiconductor layer but higher doping density compare with said second conductive type semiconductor layer; and the said second well region surround the said first well' region at first distance, P+ at the left side of fig. 6, and form lateral PN junction and the said first well region to said second conductive type semiconductor layer form vertical PN junction, N+ to P-EPI Layer,

limitations from claim 6: further comprising: forming latch up preventing deep well, a deep well is formed at third center depth and first thickness in said second conductive semiconductor layer below standard N well and standard P well with said second conductive type doping in sensor accessory circuit area to prevent latch up happen, wherein applying the merger doctrine, Lee uses the top part of the well as the first well and the lower part as the latch-up preventing well;

limitations from claim 9: wherein the said first conductive type semiconductor is N type substrate, the said conductive second type semiconductor material layer is a P- type epitaxial layer, p. 3, ¶ 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3, 4, 5, 7, 10, 11, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee as applied to claims 1, 6, 9 above, and further in view of Applicant's Admitted Prior Art.

Lee does not specify integration of the photodetector with a CMOS configuration, AAPA does. AAPA in fig. 1, teaches the said first well region can be realized by the standard well forming in standard CMOS process, the left side of the diagram, with said first conductive type semiconductor; or realized by the standard CMOS well stacked with a deep well 110, 114 with said first conductive type semiconductor; and the said second well region can be realized by the standard well forming in standard CMOS process with said second conductive type semiconductor; or realized by the standard CMOS well stacked with a deep well with said second conductive type semiconductor, Background of Application. Although applicant suggests the type of device used by Lee would not typically be compatible, the configuration of Lee, fig. 6 has similar layer configurations to the photodiode of fig. 1. Further atypical configuration, does not rule out the configuration entirely.

Lee teaches limitations from claim 2: the first conductive type semiconductor substrate and the second conductive type semiconductor layer are connecting to different voltage and the said PN junction is reversing biased, in fig. 6, the symbol for the voltage difference is drawn on the bottom and to the right of the diagram for reverse biasing, and AAPA also teaches reverse biasing on p.1 , ¶ 2, of the Background. The AAPA gives motivation on p. 2, ¶ 3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining AAPA's process with Lee's invention would have been beneficial because It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining AAPA's process with Lee's invention would have been beneficial because the CMOS provides logic control circuits.

For claims 4, 5, 7, 13, and 14, Lee does not specify the distances between, the depth, the thicknesses, and the doping densities, of his regions, but the practitioner may optimize these parameters.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More

particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmischer 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claims 8, 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee as applied to claims 1, 6, 9 above, and further in view of Nakashiba, U.S. Patent No. 6,472,698.

Lee does not specify planarizing a top oxide, but Nakashiba does. Nakashiba teaches, in fig. 4B, wherein the said first conductive type semiconductor is P type substrate 1, the said second conductive type semiconductor material layer is a N- type epitaxial layer, 4, a well-known practice to invert the charging types for device manufacturing, col. 1, line 61 - col. 2, line 14; growing a top oxide layer, referred to as 34 and 44, and after growing a top oxide layer, carrying out a process of chemical mechanical polishing (CMP), col. 4, lines 1-15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that

combining Nakashiba's process with Lee's invention would have been beneficial because it has the correct height and flat surface to form microlens 35.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

12 May 2004
WB